ACT-317

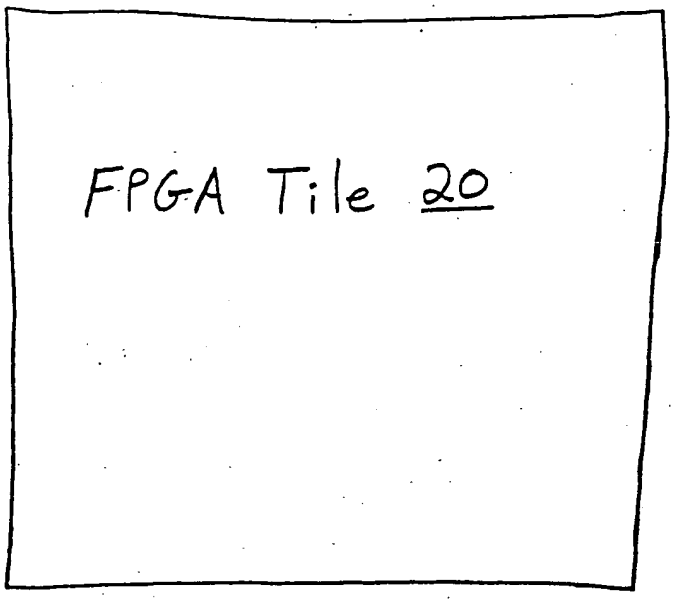

FIG. 1

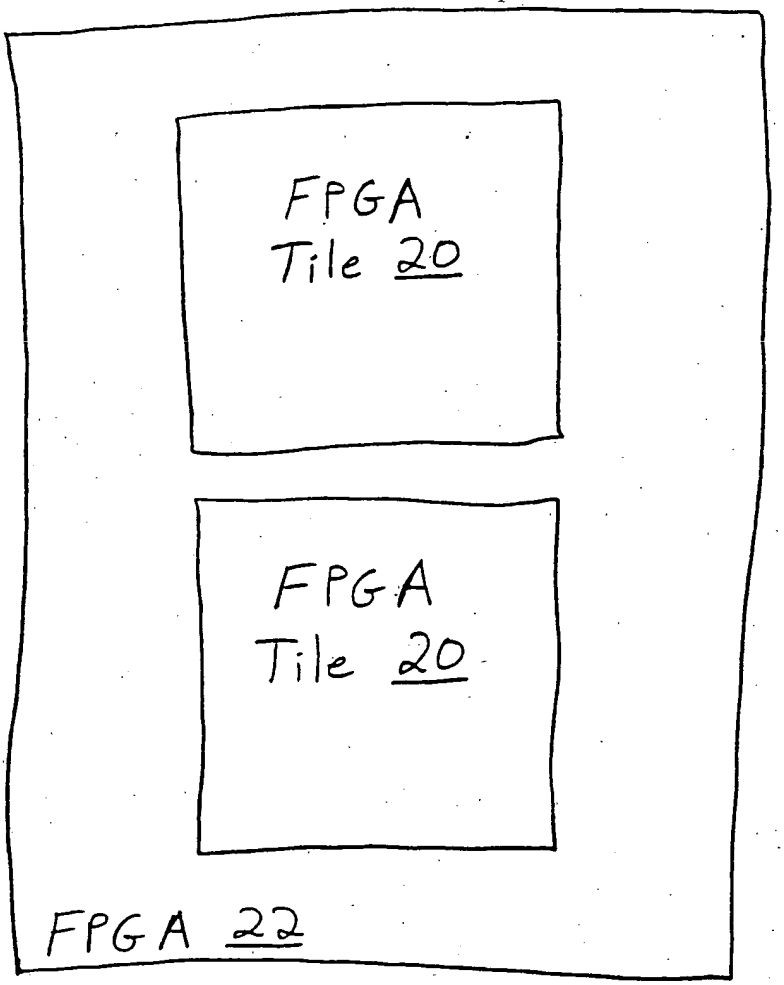

FIG. 2

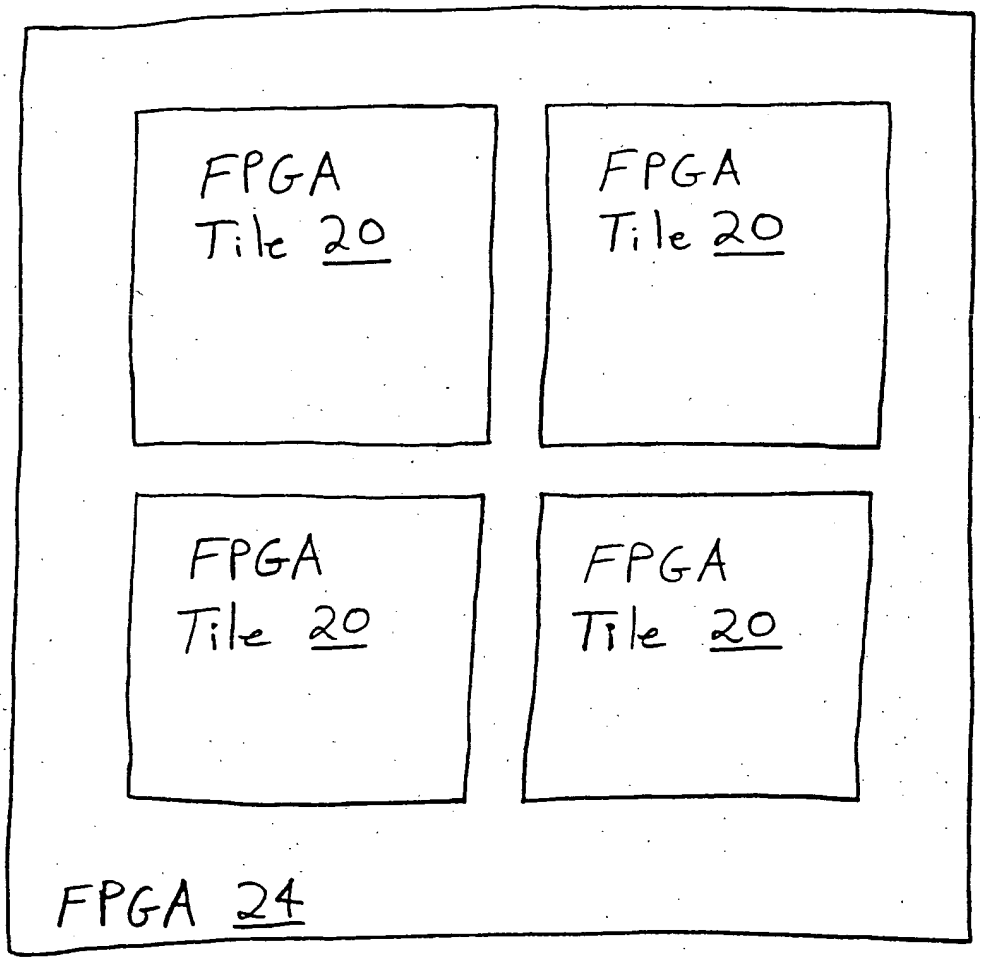

FIG. 3A

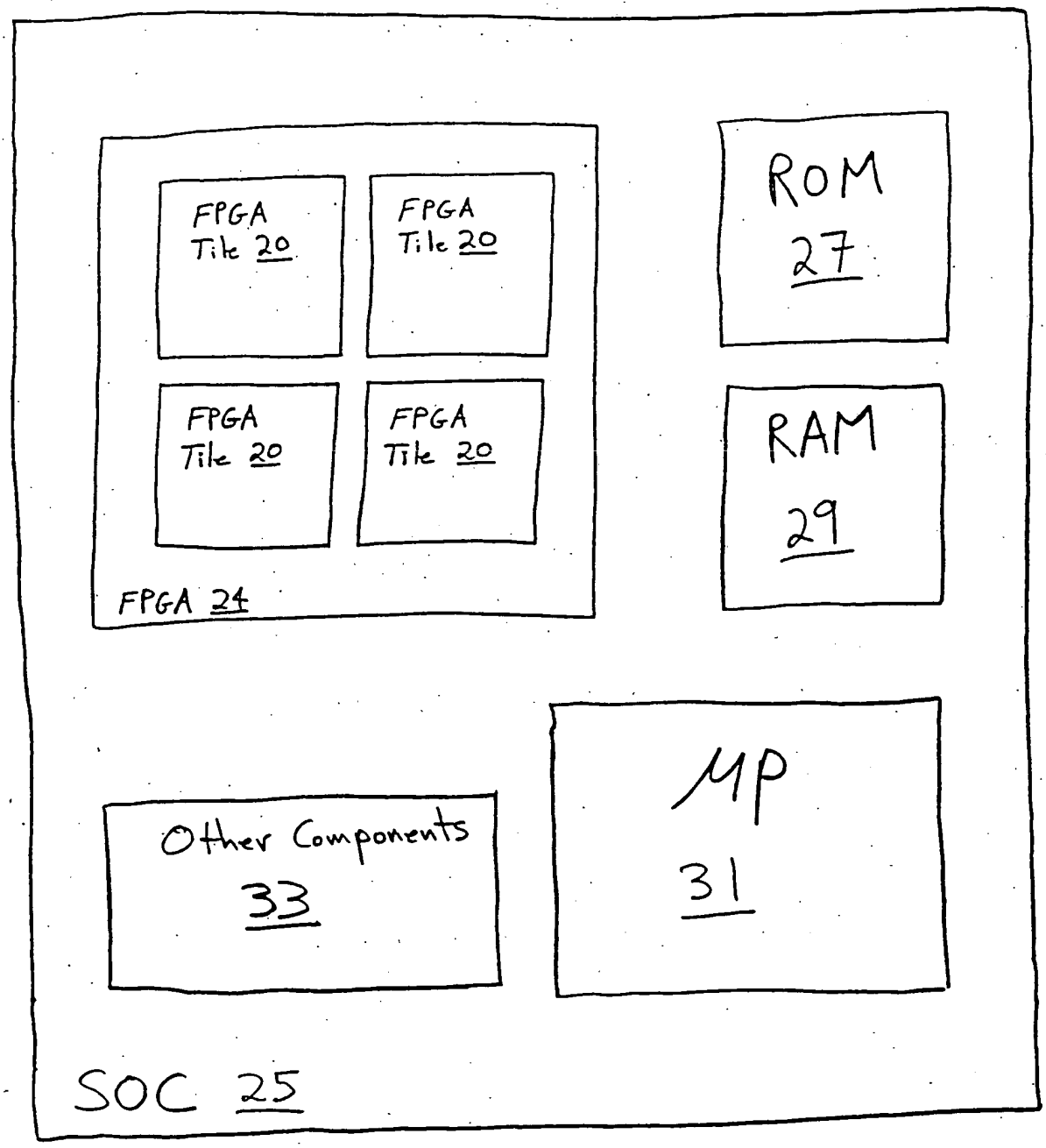

FIG. 3B

EL 85 89 79 398 US

ACT-317

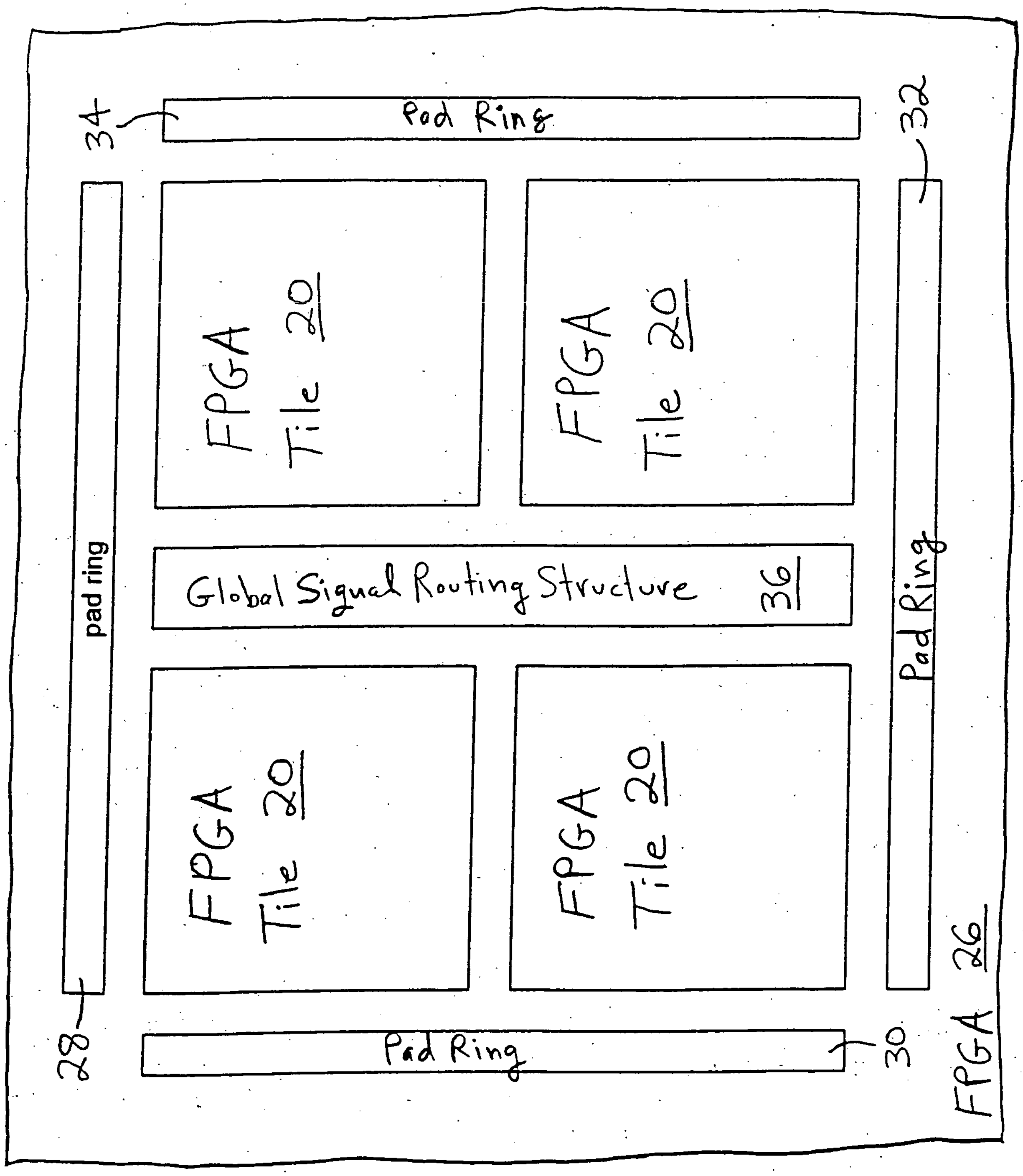

FIG. 4

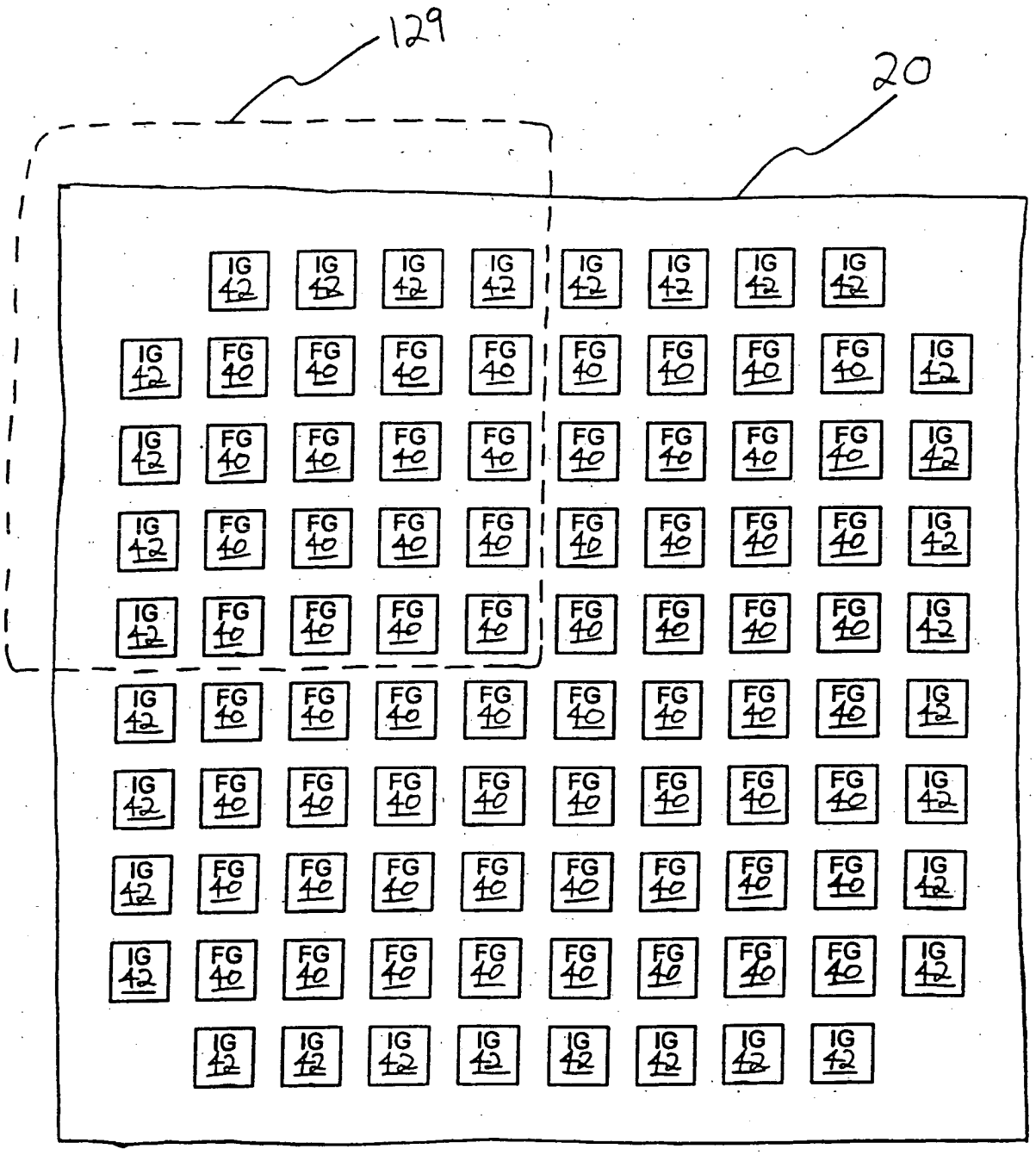

FIG. 5

ACT-317

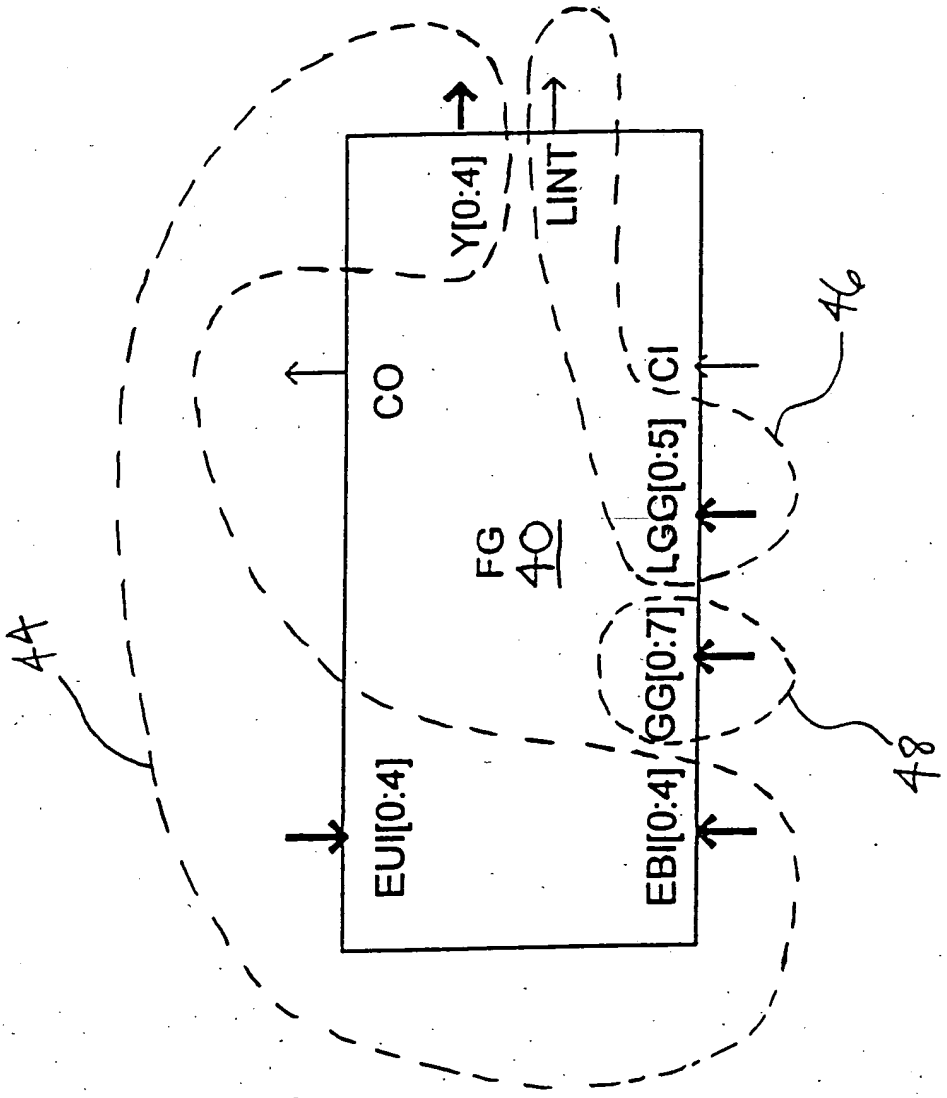

FIG. 6

ACT-317

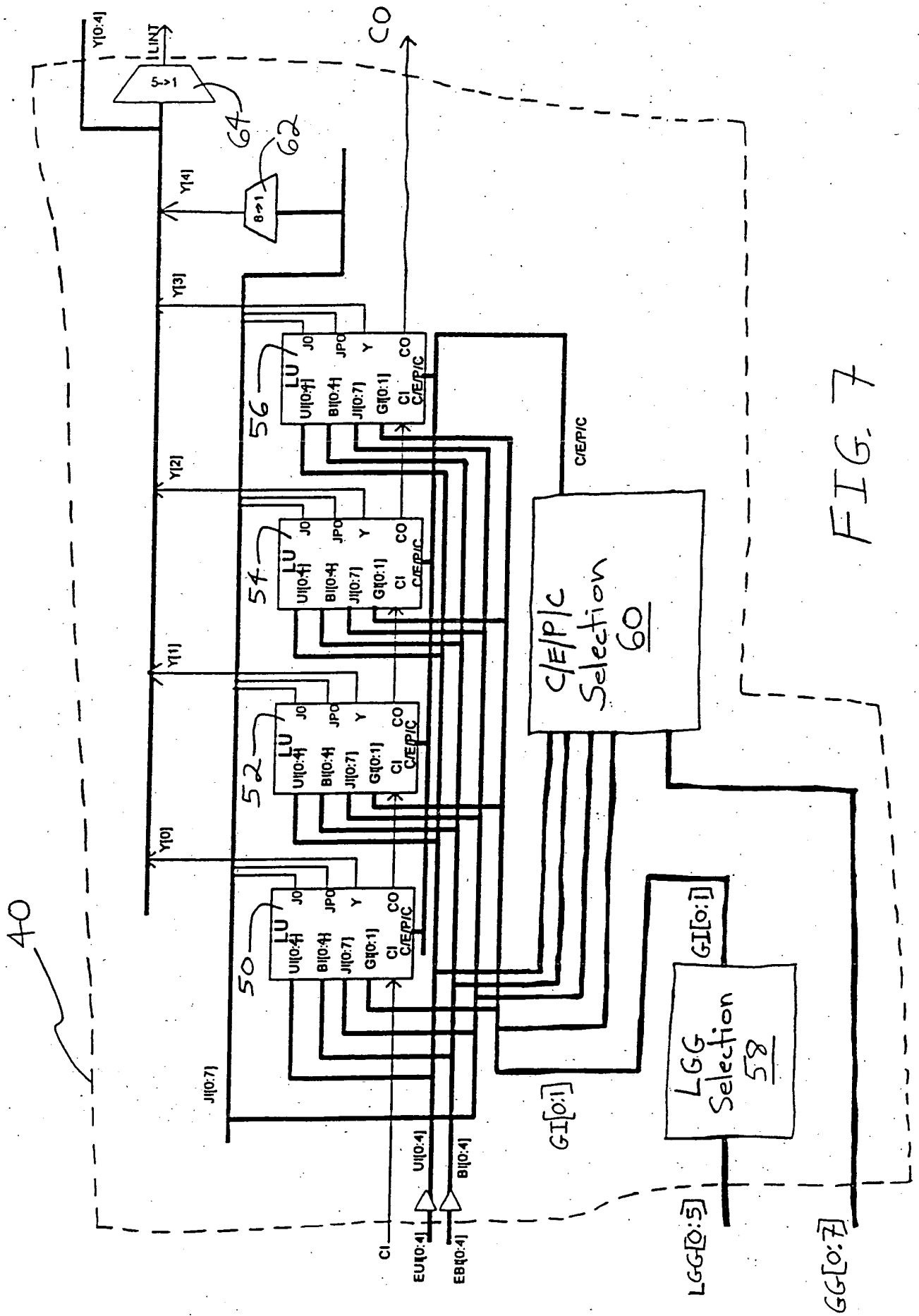

FIG. 7

ACT-317

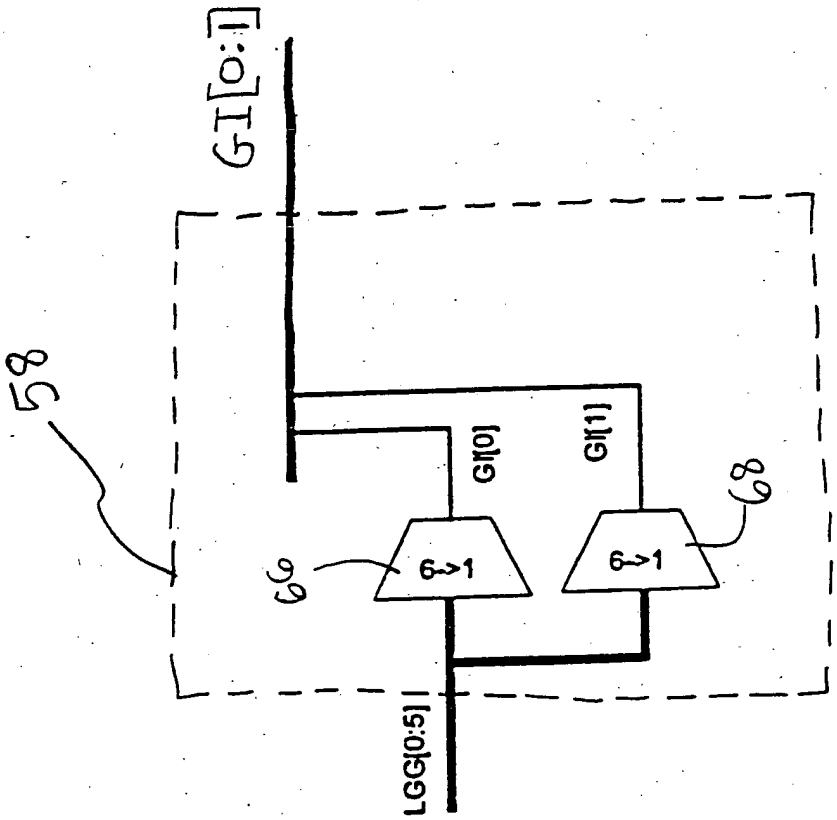

FIG. 8

ACT-317

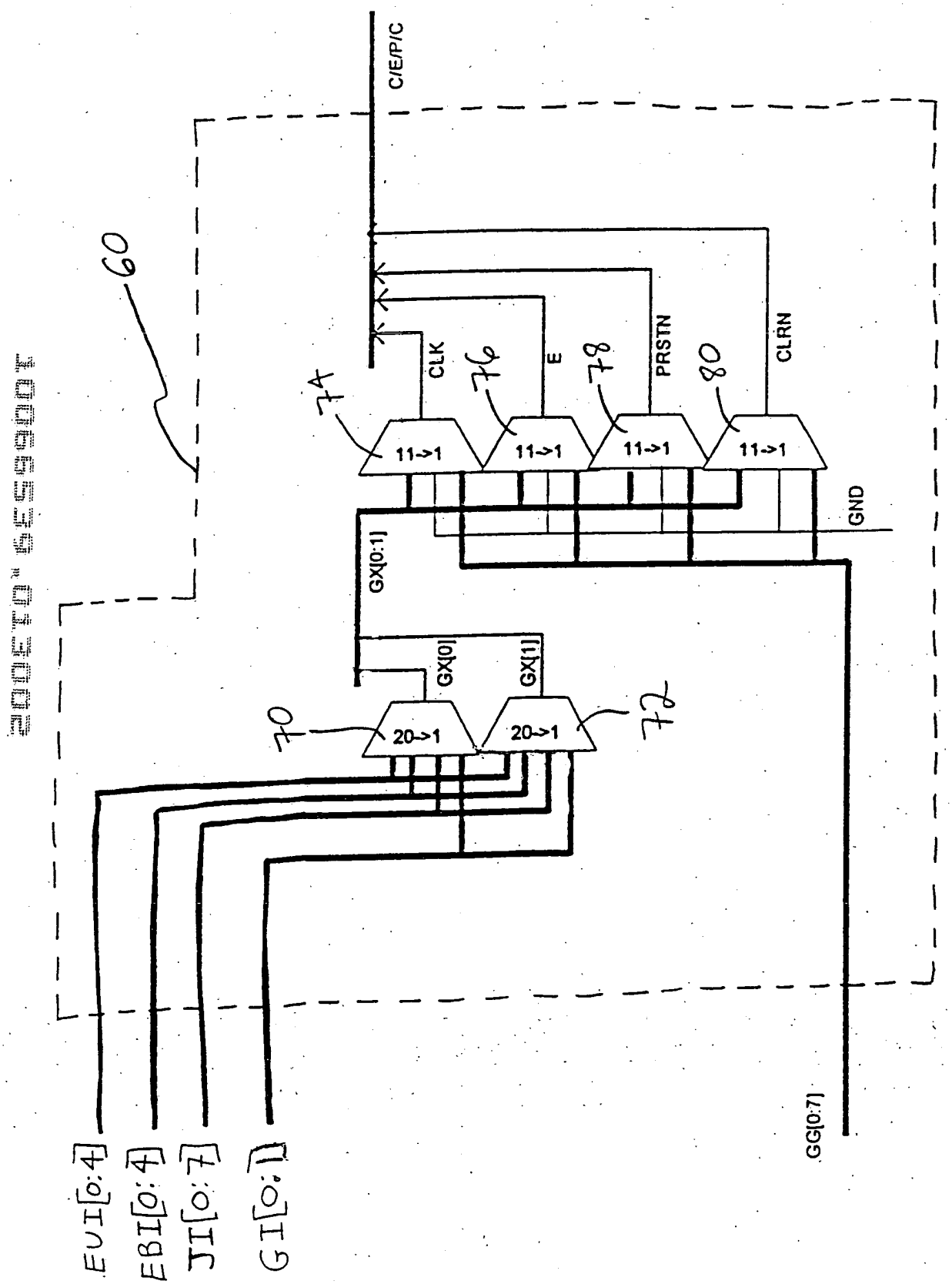
C/E/P/C
CLK
E
PRSTN
CLRN
74
76
78
80
11->1
11->1
11->1
11->1
GND
GX[0:1]
GX[0]
GX[1]
70
20->1
20->1
72
EUI[0:4]
EBI[0:4]
JI[0:7]
GI[0:1]
GG[0:7]
60

FIG. 9

ACT-317

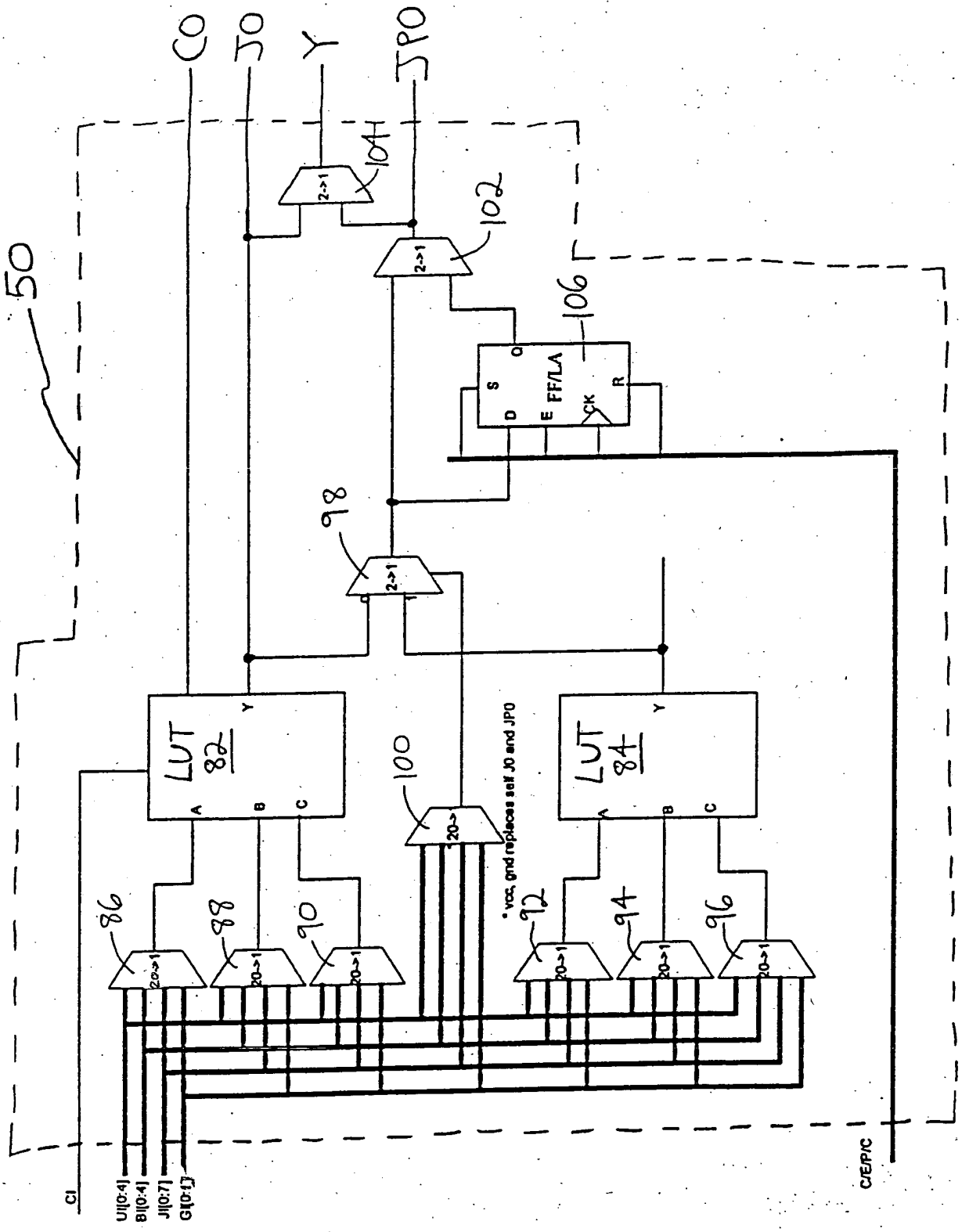

FIG. 10

ACT-317

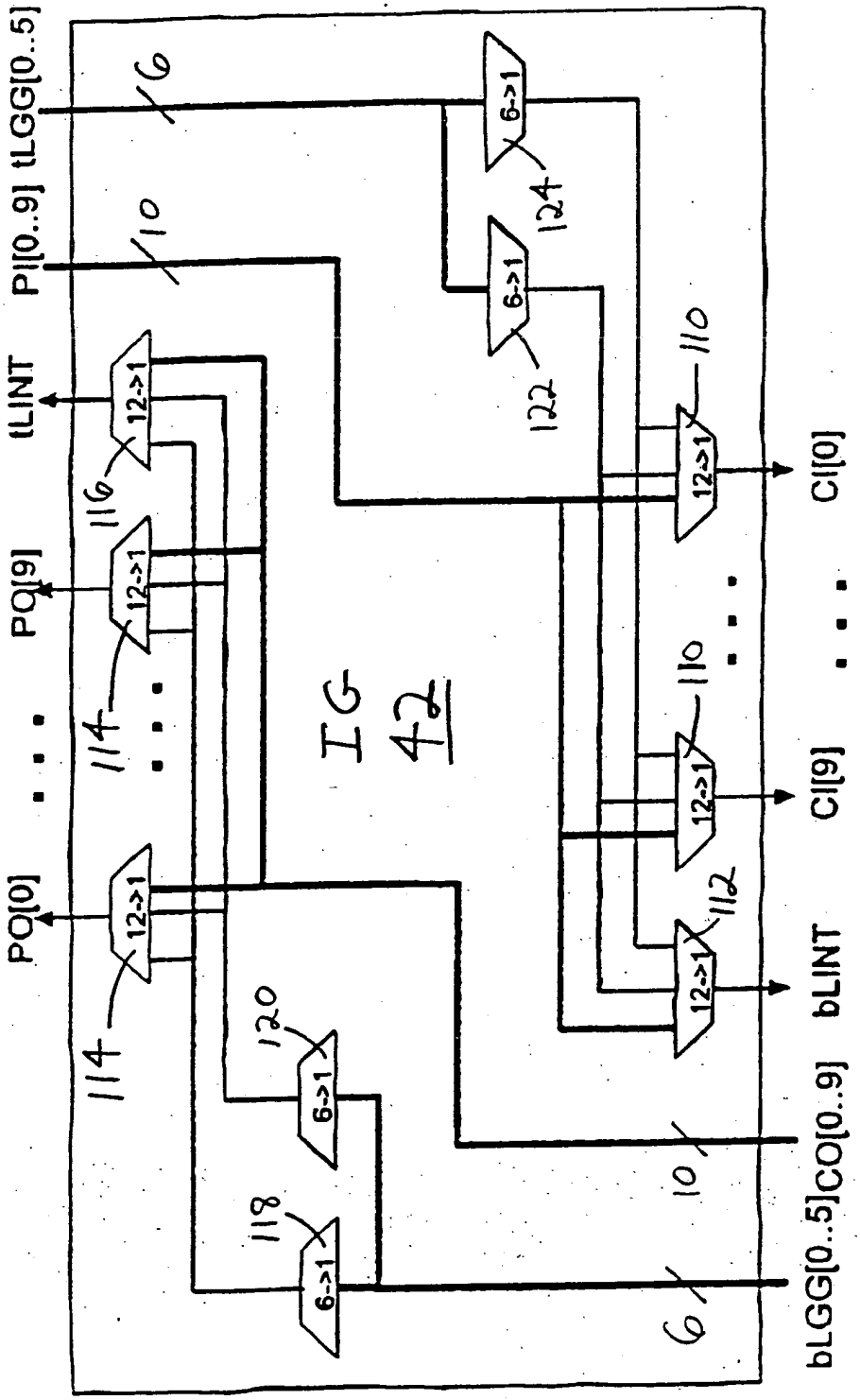

FIG. 11

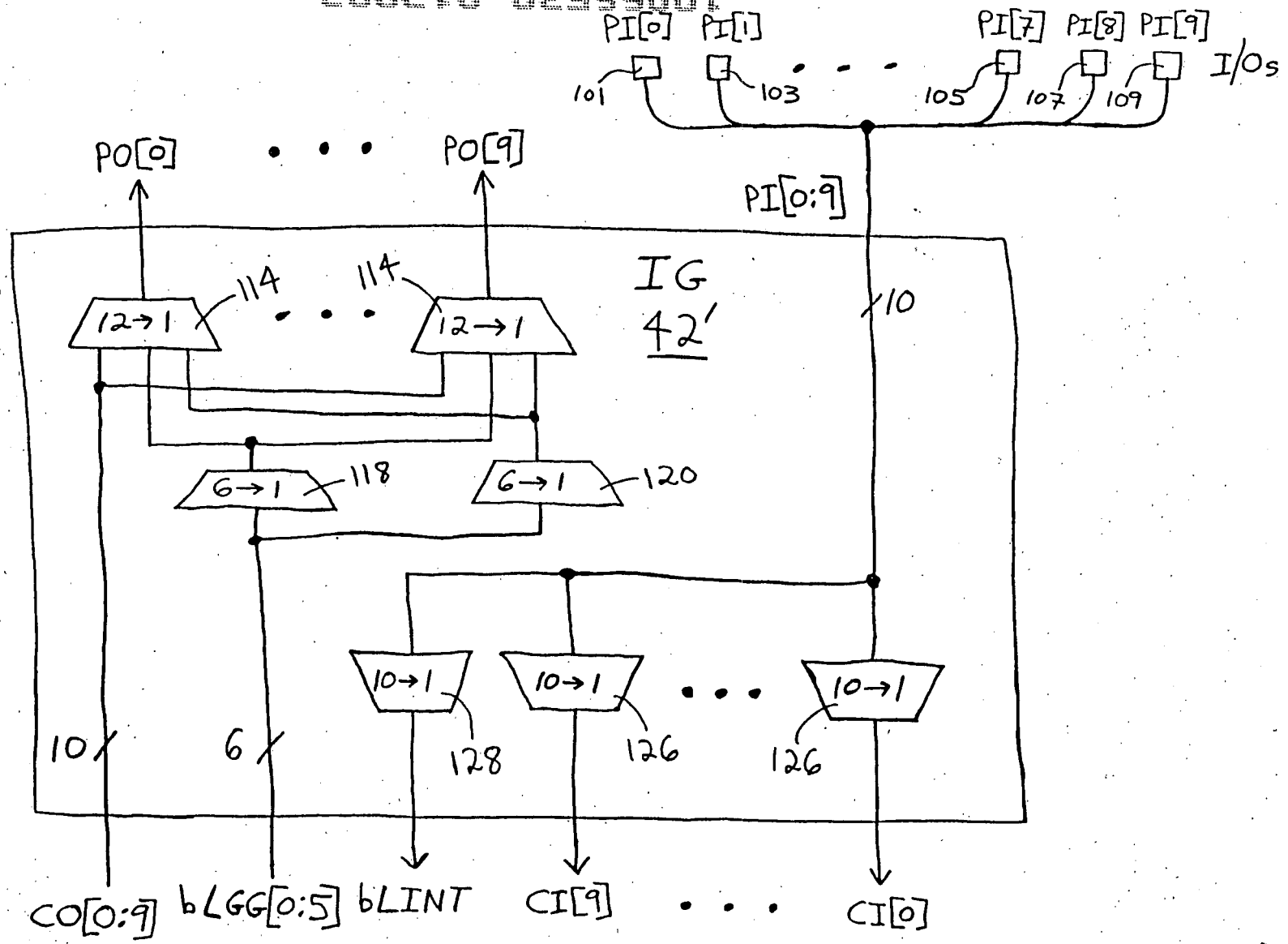

FIG. 12

ACT-317

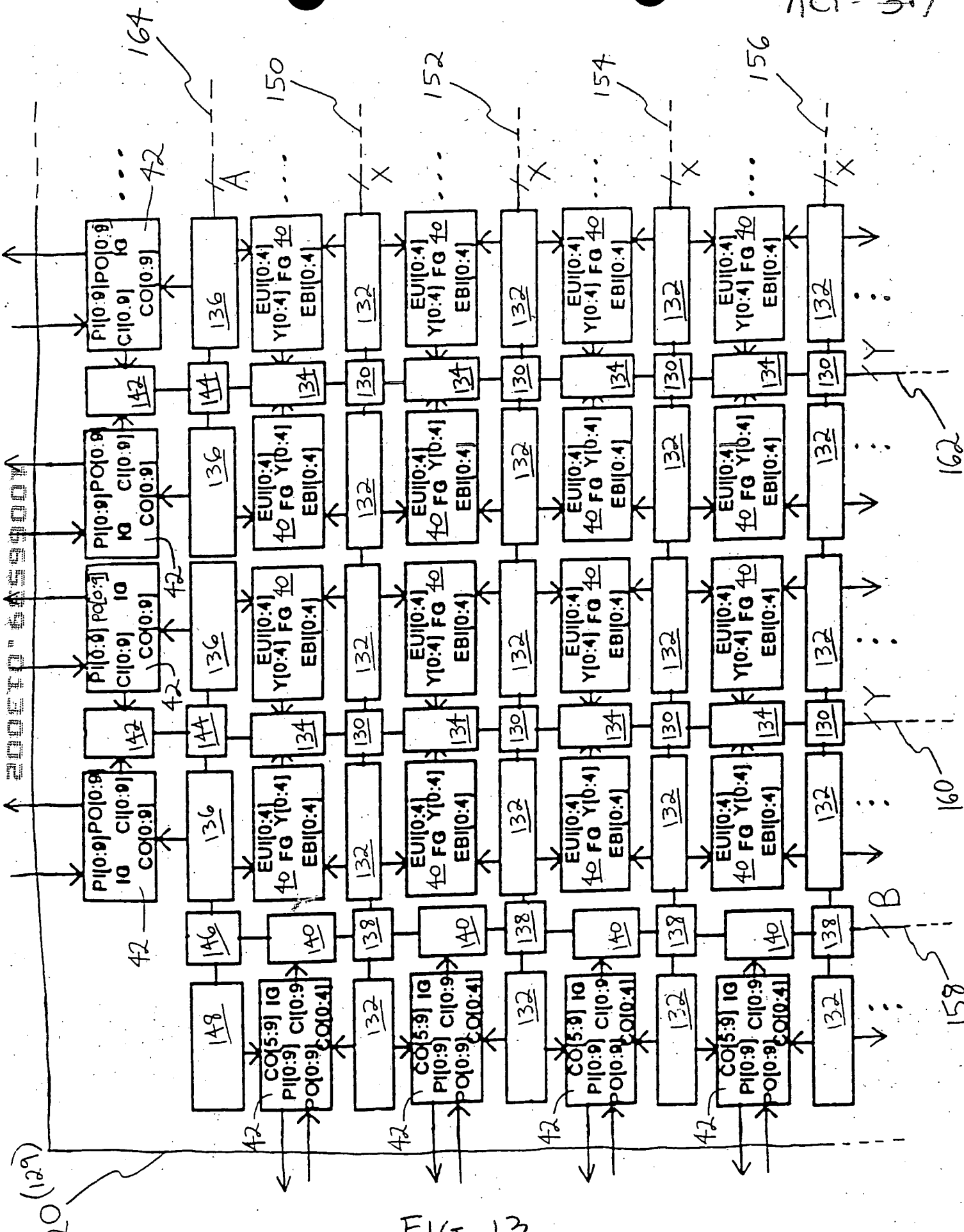

FIG. 13

ACT-317

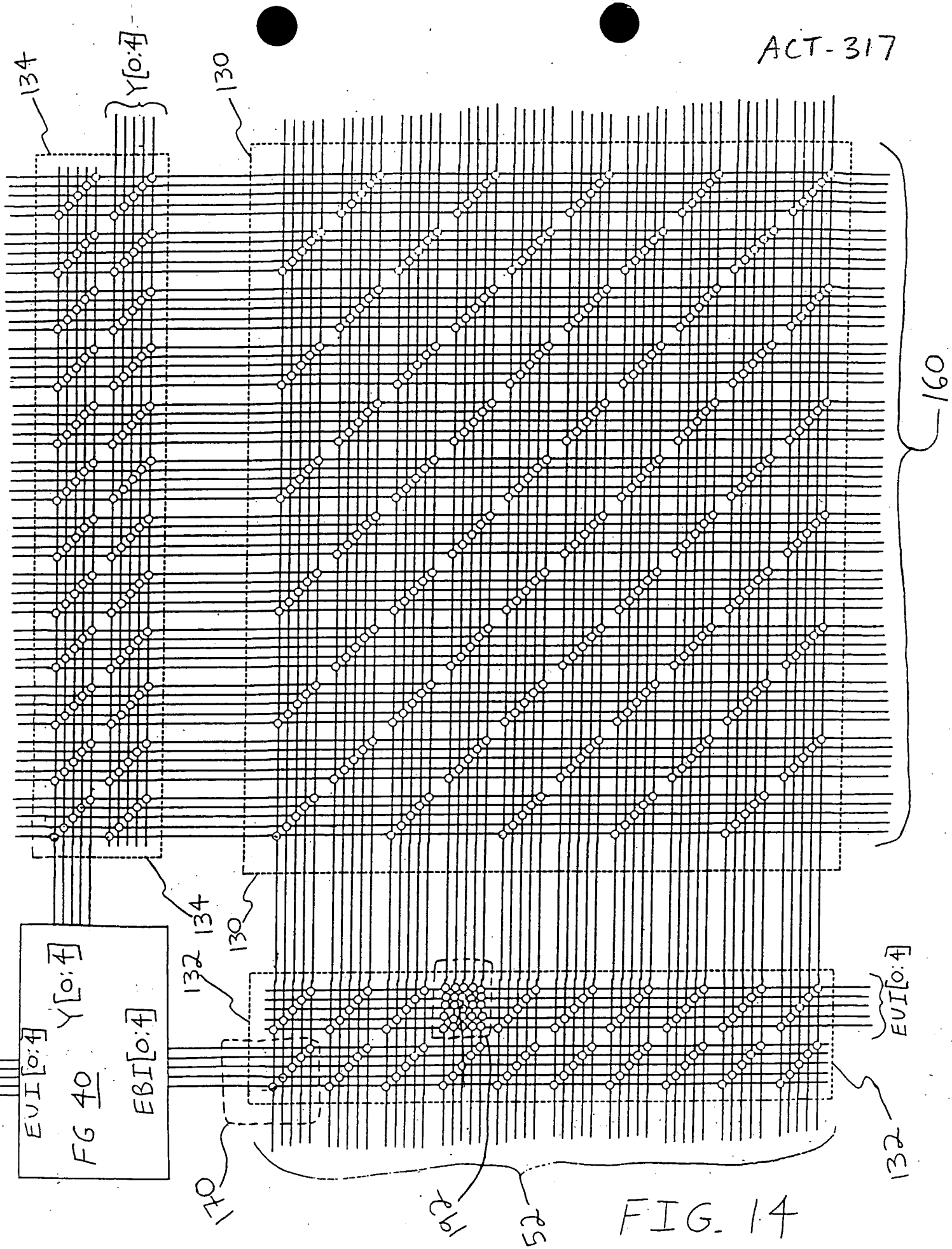

FIG. 40

FIG. 14

ACT-317

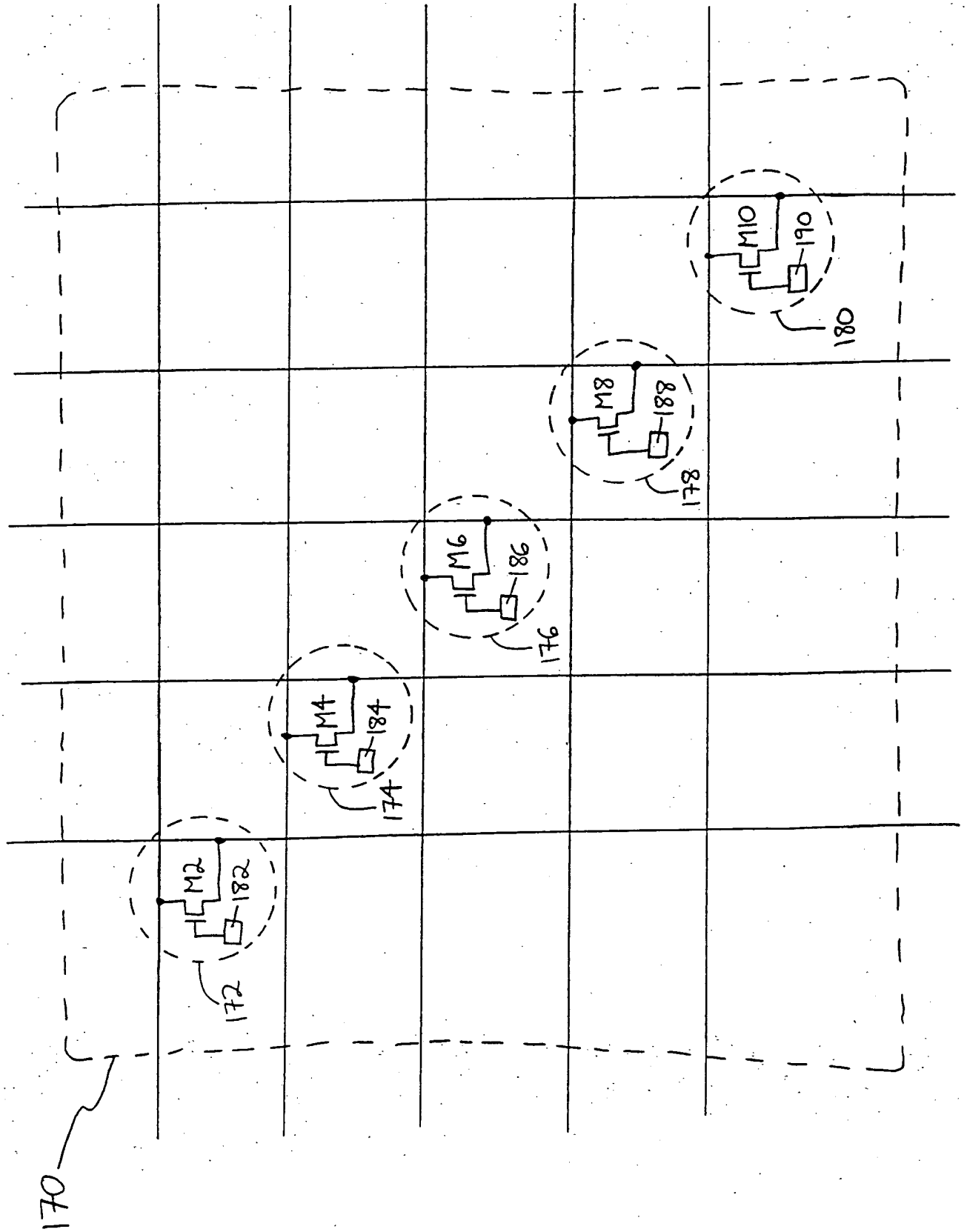

FIG. 15

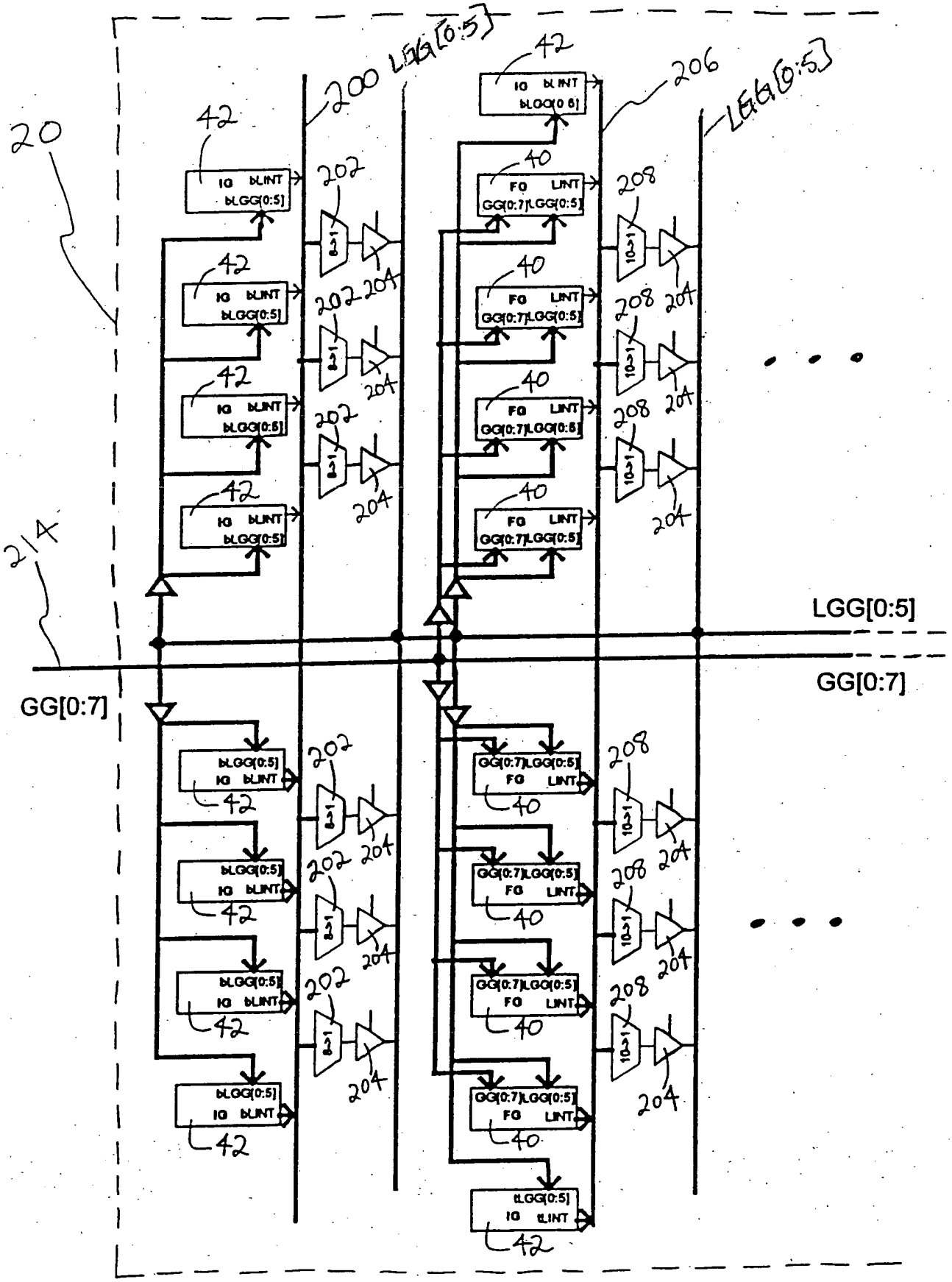
20
200
LGG[0:5]
206
LGG[0:5]
214
LGG[0:5]
GG[0:7]
GG[0:7]
42
40
202
204
208
IG bLINT
bLGG[0:5]
FG LINT
GG[0:7]LGG[0:5]
bLGG[0:5]
IG bLINT
GG[0:7]LGG[0:5]
FG LINT
tLGG[0:5]
IG tLINT
2:1
10:1

FIG. 16A

ACT-317

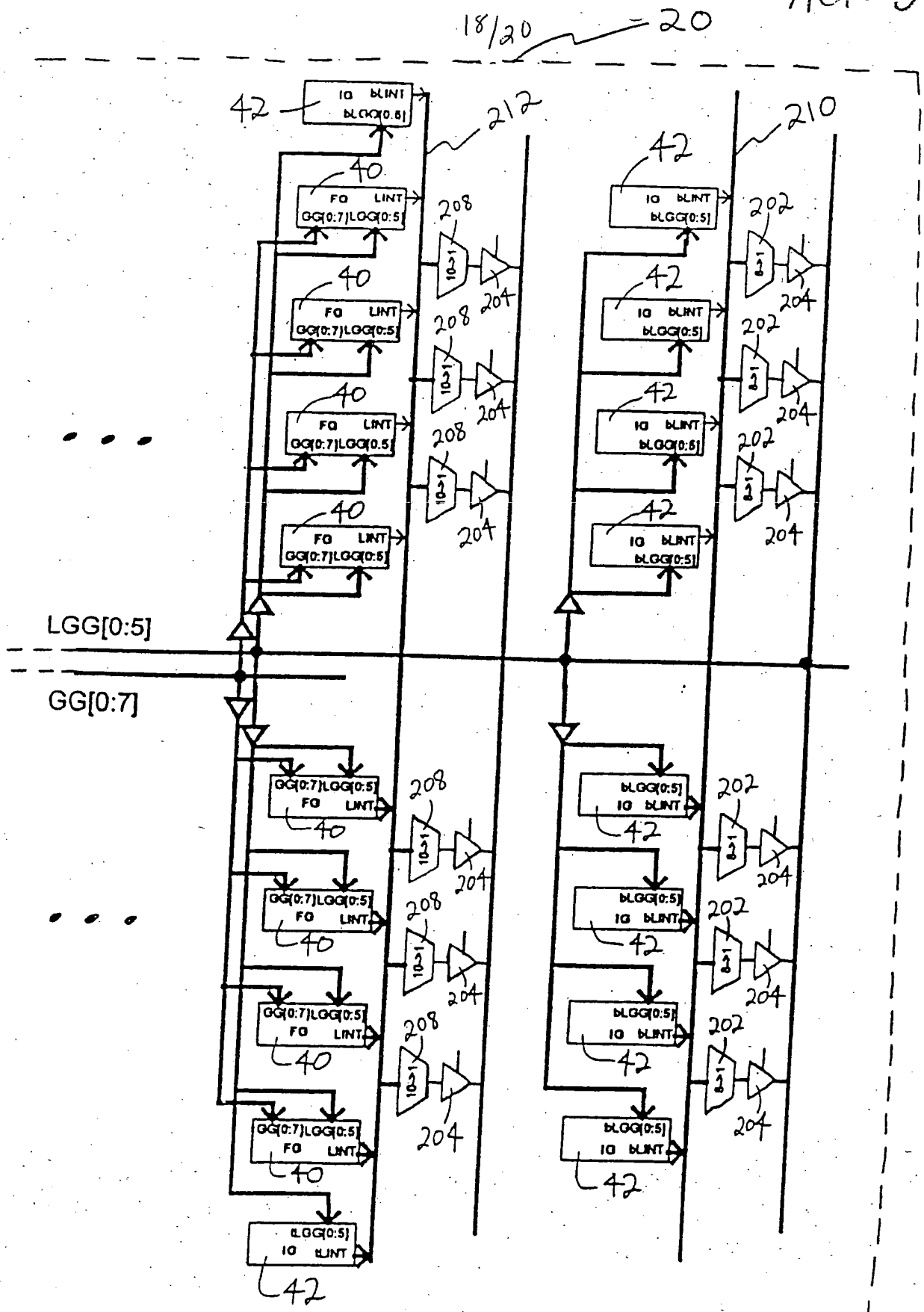

FIG. 16B

ACT-317

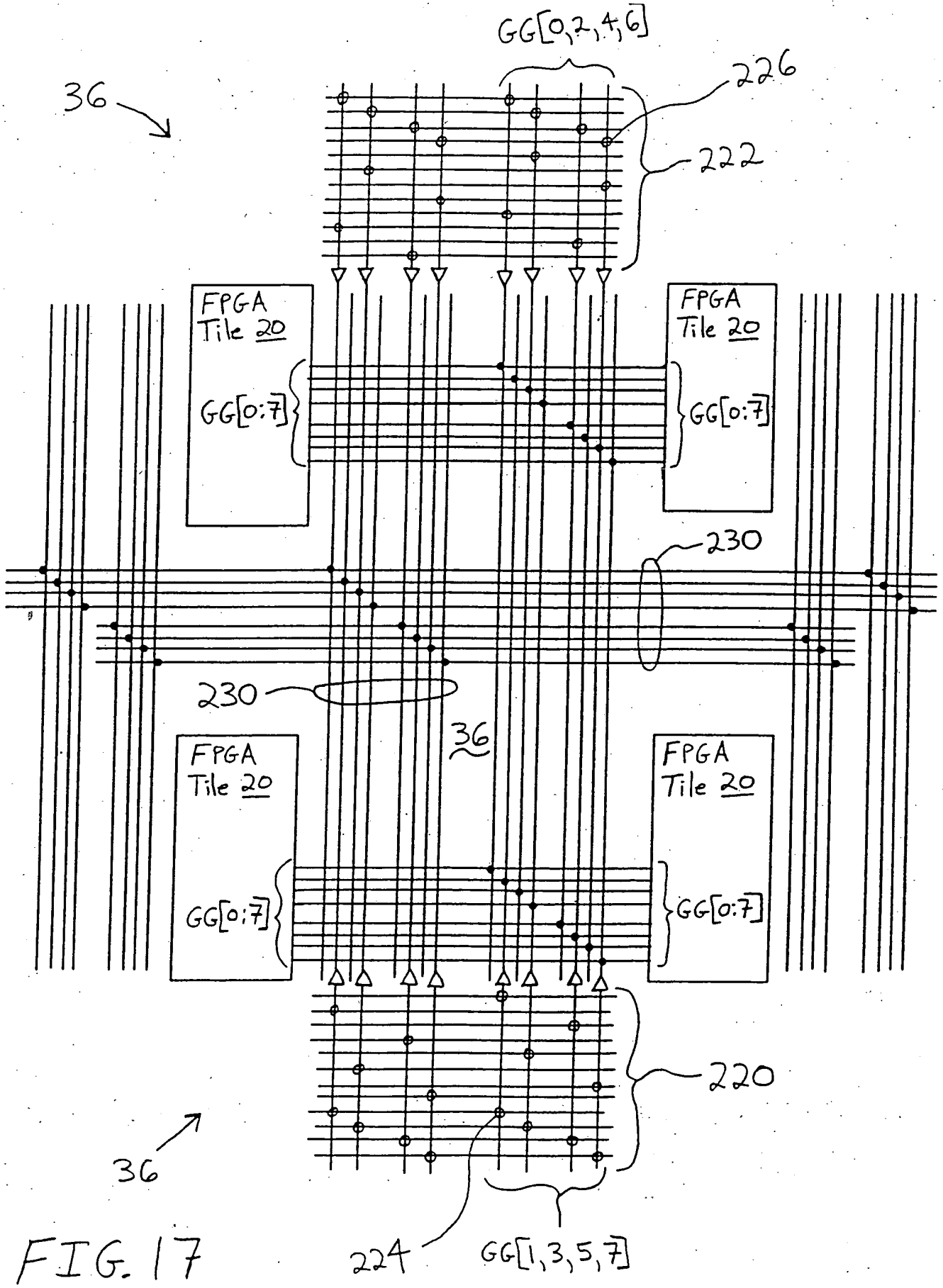

FIG. 17

ACT-317

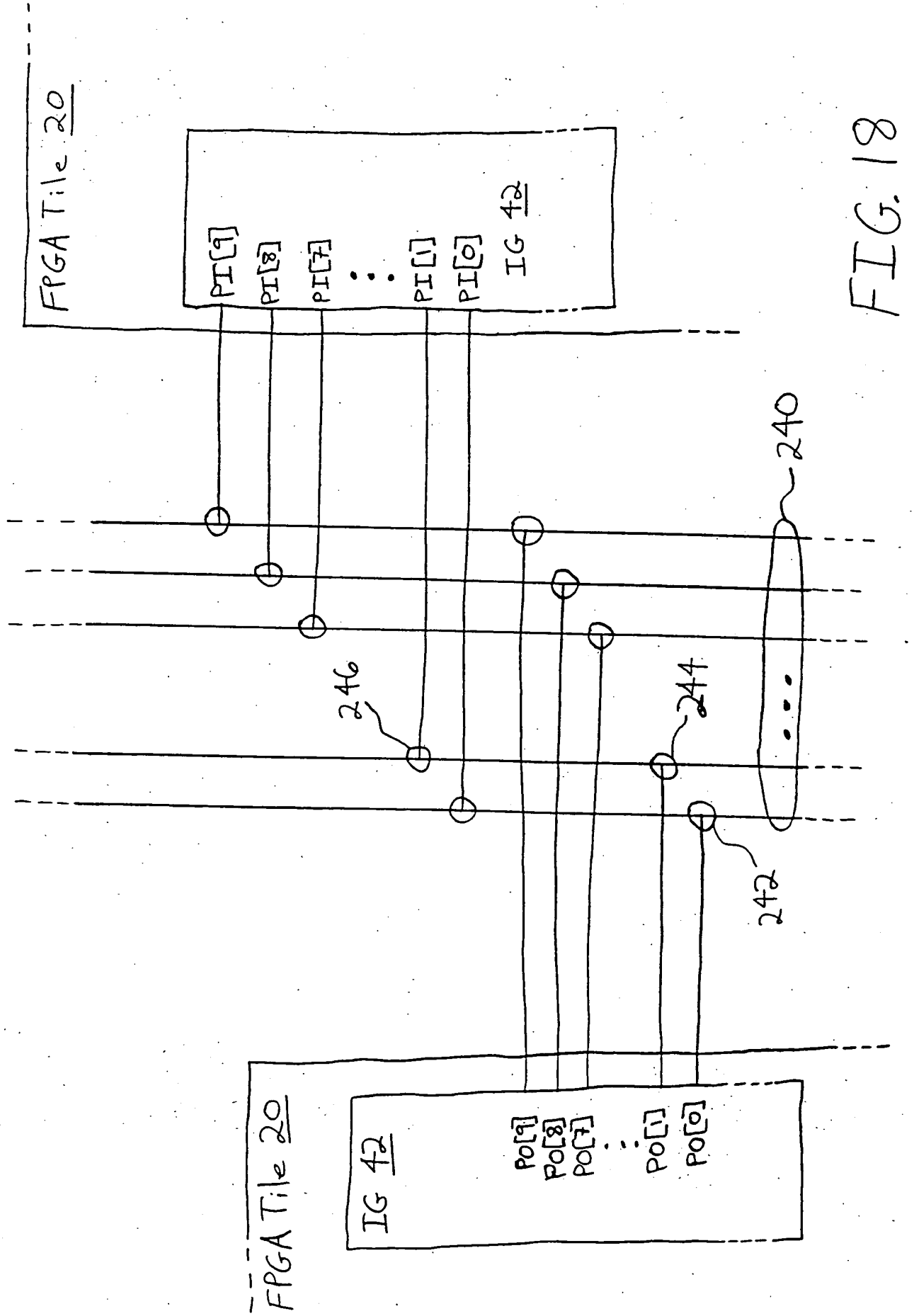

FIG. 18

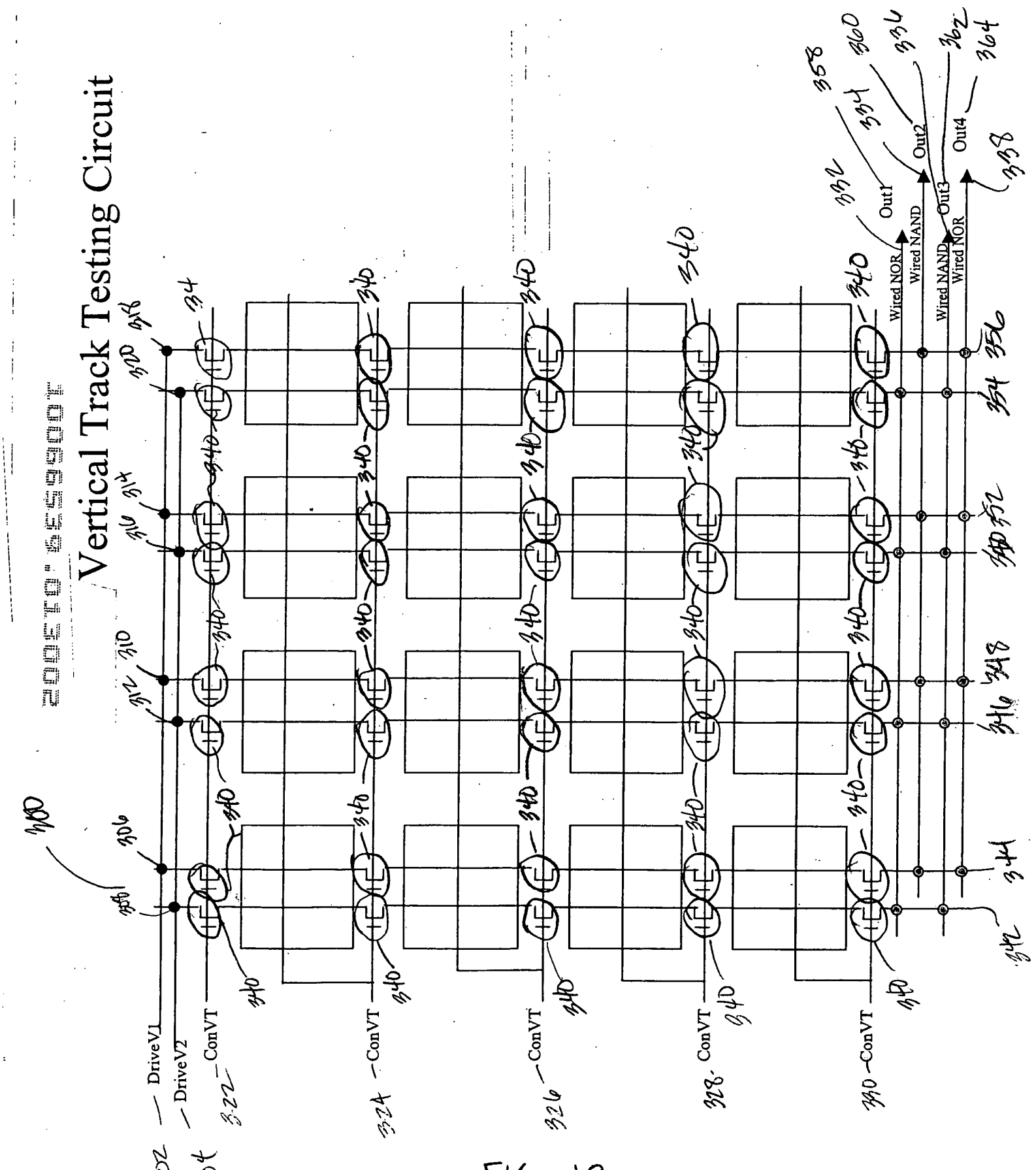
Vertical Track Testing Circuit
DriveV1
DriveV2
ConVT
Wired NOR
Wired NAND
Wired NAND
Wired NOR
Out1
Out2
Out3
Out4

FIG. 19

ACT-317

Truth Table

DriveV1	DriveV2	Out1	Out2	Out3	Out4
0	0	1	1	1	1
0	1	1	0	1	0
1	0	0	1	0	1
1	1	0	0	0	0

Fig. 20

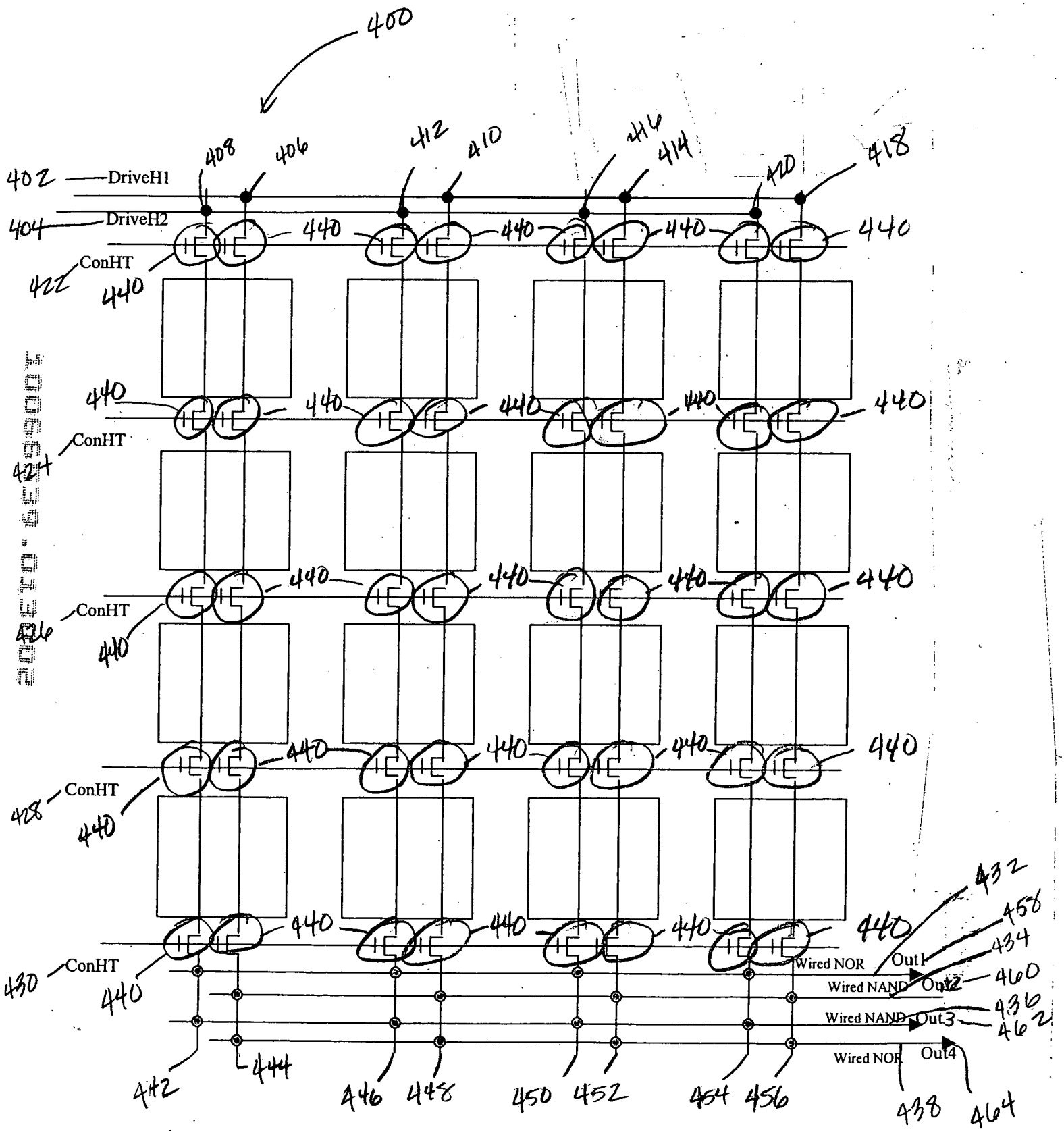
400
402
DriveH1
404
DriveH2
406
408
410
412
414
416
418
420
422
ConHT
424
ConHT
426
ConHT
428
ConHT
430
440
Wired NOR
Out1
Wired NAND
Out2
Wired NAND
Out3
Wired NOR
Out4
432
434
436
438
442
444
446
448
450
452
454
456
458
460
462
464

FIG. 21

ACT-317

Truth Table

DriveH1	DriveH2	Out1	Out2	Out3	Out4
0	0	1	1	1	1
0	1	1	0	1	0
1	0	0	1	0	1
1	1	0	0	0	0

FIG. 22